

## Y86 Instruction Set Reference

Instruction	Byte offset from PC										Instruction	Byte offset from PC															
	0	1	2	3	4	5	6	7	8	9		0	1	2	3	4	5	6	7	8							
halt	0	0											jXX Dest	7	fn	Dest											
nop	1	0											call Dest	8	0	Dest											
cmovXX rA, rB	2	fn	rA	rB											ret	9	0										
irmovq V, rB	3	0	f	rB	V										pushq rA	a	0	rA	f								
rmmovq rA, D(rB)	4	0	rA	rB	D										popq rA	b	0	rA	f								
mrmmovq D(rB), rA	5	0	rA	rB	D										iotrap id	c	id										
OPq rA, rB	6	fn	rA	rB																							

<b>cmovXX:</b>	
rrmovq	20
cmovle	21
cmovl	22
cmove	23
cmovne	24
cmovge	25
cmovg	26

<b>OPq:</b>	
addq	60
subq	61
andq	62
xorq	63

<b>jXX:</b>	
jmp	70
jle	71
jl	72
je	73
jne	74
jge	75
jg	76

<b>Trap IDs:</b>	
charout	0
charin	1
decout	2
decin	3
strout	4
flush	5

<b>Registers:</b>			
%rax <sup>+</sup>	0	%rbp <sup>*</sup>	5
%rcx <sup>+</sup>	1	%rsi <sup>+</sup>	6
%rdx <sup>+</sup>	2	%rdi <sup>+</sup>	7
%rbx <sup>*</sup>	3	%r8-%r11 <sup>+</sup>	
%rsp	4	%r12-%r14 <sup>*</sup>	

<sup>+</sup> indicates caller-save  
<sup>\*</sup> indicates callee-save

<b>Args:</b>		<b>Status Codes:</b>	
%rdi		AOK	1
%rsi		HLT	2
%rdx		ADR	3
%rcx		INS	4
%r8			
%r9			

In the following semantics, **PC**, **STAT**, and **CC** refer to the program counter, status code, and condition codes of the CPU.

Stage	HALT	NOP	cmovXX	IRMOVQ
Fch	icode:ifun ← M <sub>1</sub> [PC]  valP ← PC + 1	icode:ifun ← M <sub>1</sub> [PC]  valP ← PC + 1	icode:ifun ← M <sub>1</sub> [PC] rA:rB ← M <sub>1</sub> [PC+1]  valP ← PC + 2	icode:ifun ← M <sub>1</sub> [PC] rA:rB ← M <sub>1</sub> [PC+1] valC ← M <sub>8</sub> [PC+2] valP ← PC + 10
Dec			valA ← R[rA]	
Exe	STAT ← HLT		valE ← valA Cnd ← Cond(CC, ifun)	valE ← valC
Mem				
WB			Cnd ? R[rB] ← valE	R[rB] ← valE
PC	PC ← valP	PC ← valP	PC ← valP	PC ← valP
Stage	RMMOVQ	MRMOVQ	OPq	jXX
Fch	icode:ifun ← M <sub>1</sub> [PC] rA:rB ← M <sub>1</sub> [PC+1] valC ← M <sub>8</sub> [PC+2] valP ← PC + 10	icode:ifun ← M <sub>1</sub> [PC] rA:rB ← M <sub>1</sub> [PC+1] valC ← M <sub>8</sub> [PC+2] valP ← PC + 10	icode:ifun ← M <sub>1</sub> [PC] rA:rB ← M <sub>1</sub> [PC+1]  valP ← PC + 2	icode:ifun ← M <sub>1</sub> [PC]  valC ← M <sub>8</sub> [PC+1] valP ← PC + 9
Dec	valA ← R[rA] valB ← R[rB]	valB ← R[rB]	valA ← R[rA] valB ← R[rB]	
Exe	valE ← valB + valC	valE ← valB + valC	valE ← valB OP valA Set CC (ZF, SF, & OF)	Cnd ← Cond(CC, ifun)
Mem	M <sub>8</sub> [valE] ← valA	valM ← M <sub>8</sub> [valE]		
WB		R[rA] ← valM	R[rB] ← valE	
PC	PC ← valP	PC ← valP	PC ← valP	PC ← Cnd ? valC:valP
Stage	CALL	RET	PUSHQ	POPQ
Fch	icode:ifun ← M <sub>1</sub> [PC]  valC ← M <sub>8</sub> [PC+1] valP ← PC + 9	icode:ifun ← M <sub>1</sub> [PC]  valP ← PC + 1	icode:ifun ← M <sub>1</sub> [PC] rA:rB ← M <sub>1</sub> [PC+1]  valP ← PC + 2	icode:ifun ← M <sub>1</sub> [PC] rA:rB ← M <sub>1</sub> [PC+1]  valP ← PC + 2
Dec	valB ← R[RSP]	valA ← R[RSP] valB ← R[RSP]	valA ← R[rA] valB ← R[RSP]	valA ← R[RSP] valB ← R[RSP]
Exe	valE ← valB - 8	valE ← valB + 8	valE ← valB - 8	valE ← valB + 8
Mem	M <sub>8</sub> [valE] ← valP	valM ← M <sub>8</sub> [valA]	M <sub>8</sub> [valE] ← valA	valM ← M <sub>8</sub> [valA]
WB	R[RSP] ← valE	R[RSP] ← valE	R[RSP] ← valE	R[RSP] ← valE R[rA] ← valM
PC	PC ← valC	PC ← valM	PC ← valP	PC ← valP