CS 261
Fall 2016

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Sequential Circuits

Circuits

- Circuits are formed by linking gates together
  - Inputs and outputs
    - Link output of one gate to input of another
    - Some gates have multiple inputs and/or outputs
  - Combinational circuits: outputs are a boolean function of inputs
    - Not time-dependent
    - Used for computation
  - Sequential circuits: output is dependent on previous inputs
    - Time-dependent
    - Used for memory

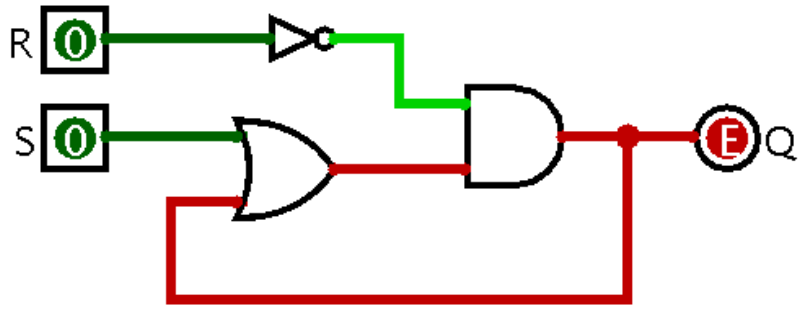
Circuit memory

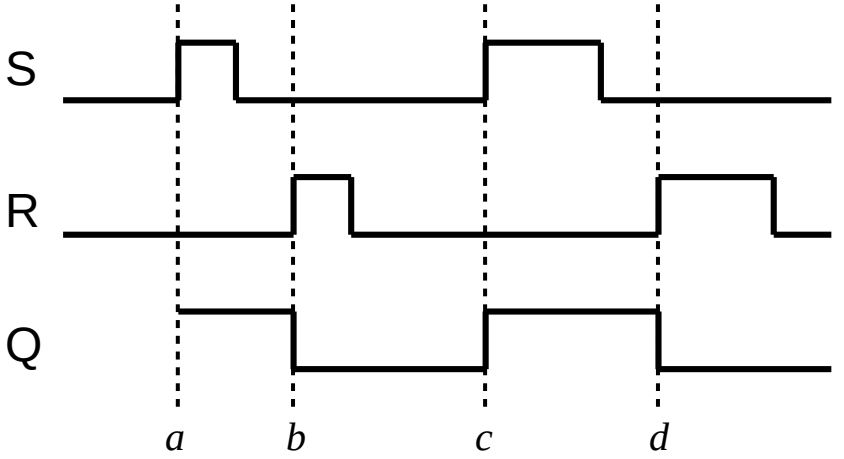
- Question: How do we make a circuit “remember” something?

Circuit memory

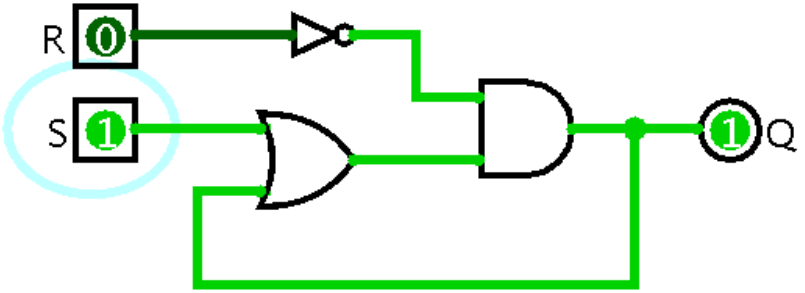
- Question: How do we make a circuit “remember” something?
  - Answer: Create a feedback loop!
  - Creates a “storage” circuit, often called a latch
  - Instead of truth table, draw a timing diagram
    - Shows how input/output signals change with respect to time
    - Given input signals in diagram, we can determine output signals

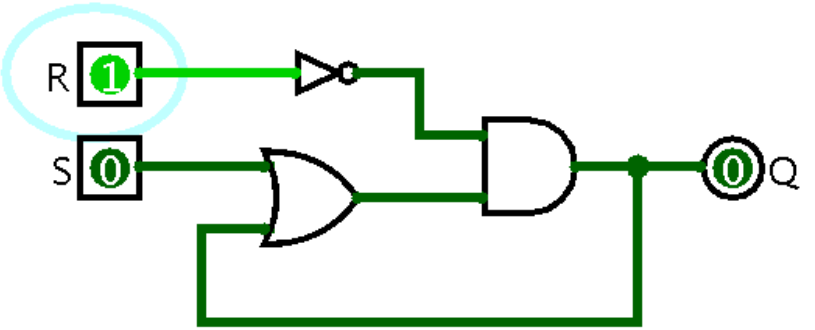
SR AND-OR latch

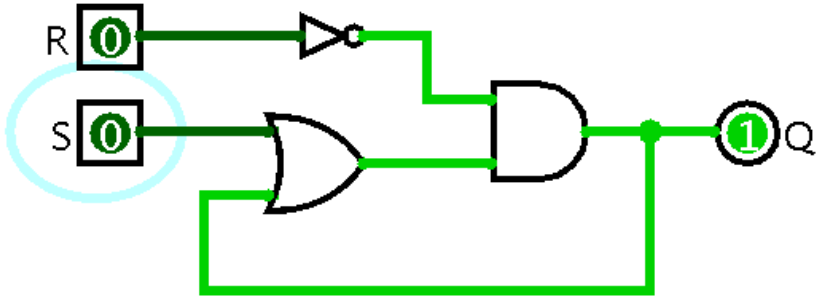


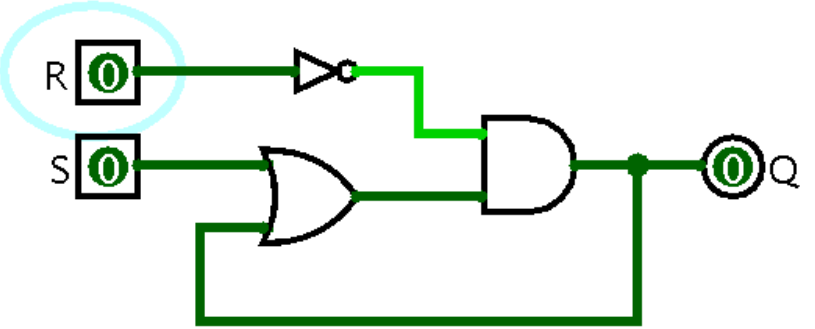


S = “set” R = “reset”

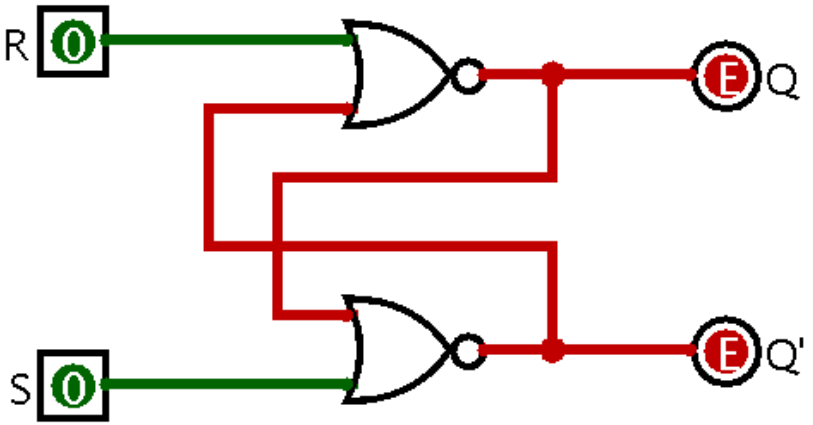


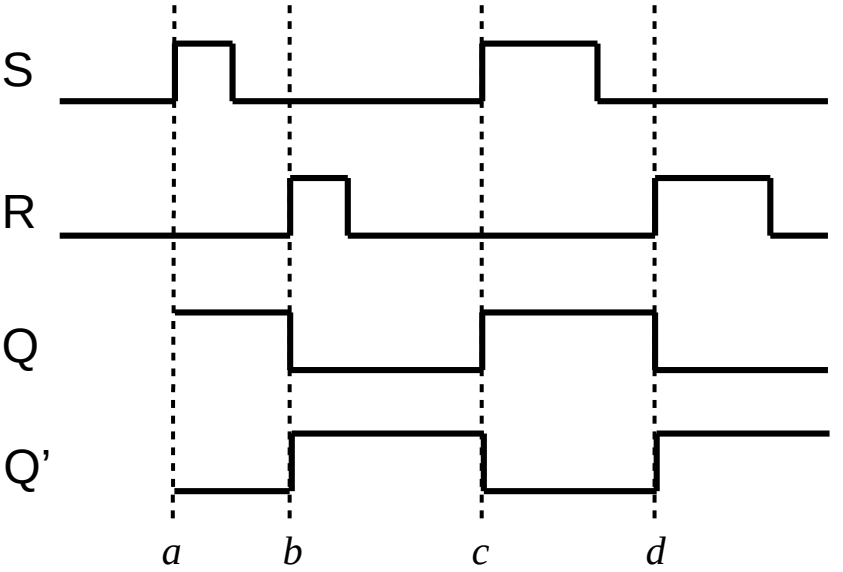


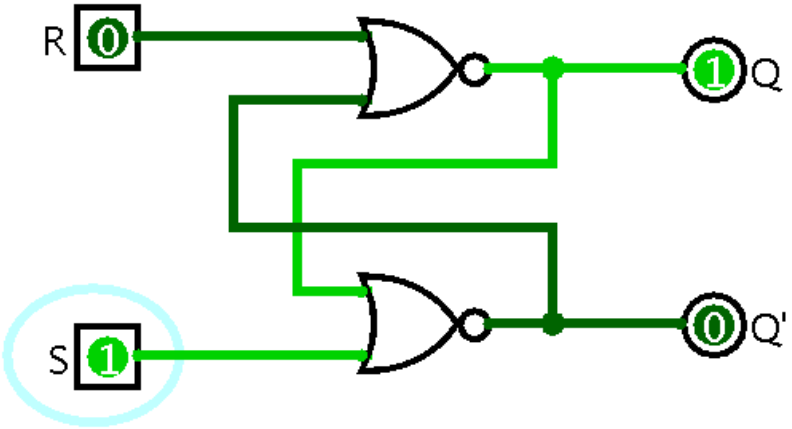


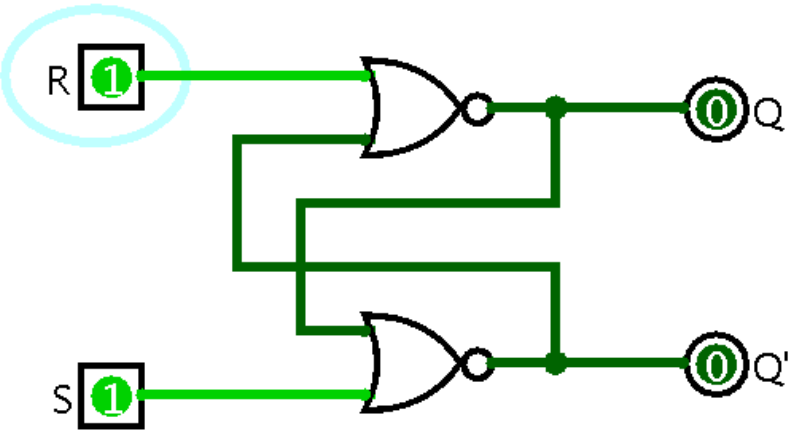


SR NOR latch



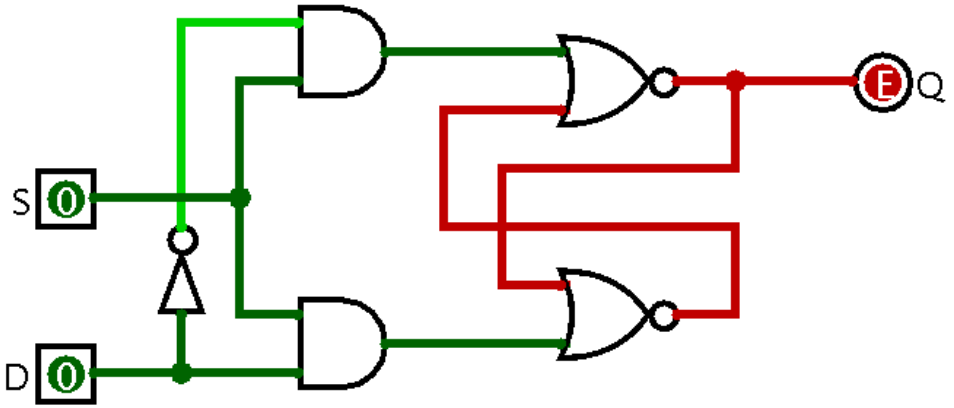


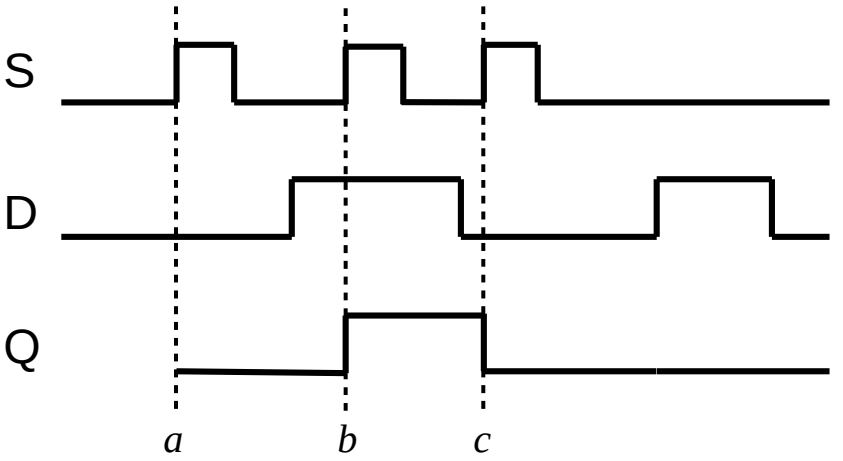




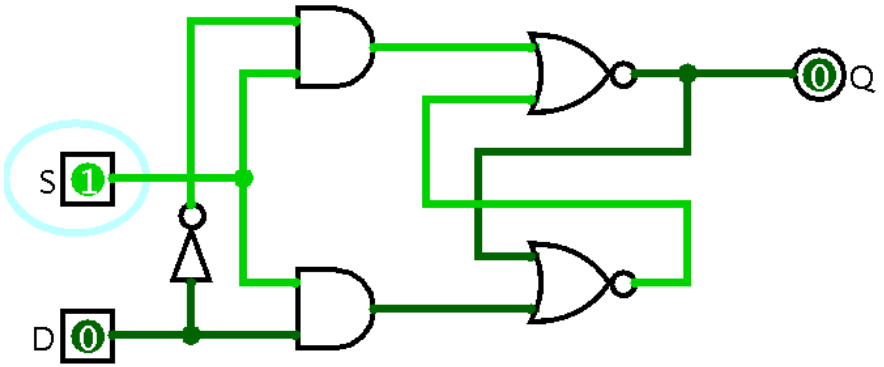
Disallow S=1, R=1 because Q’ ≠ !Q

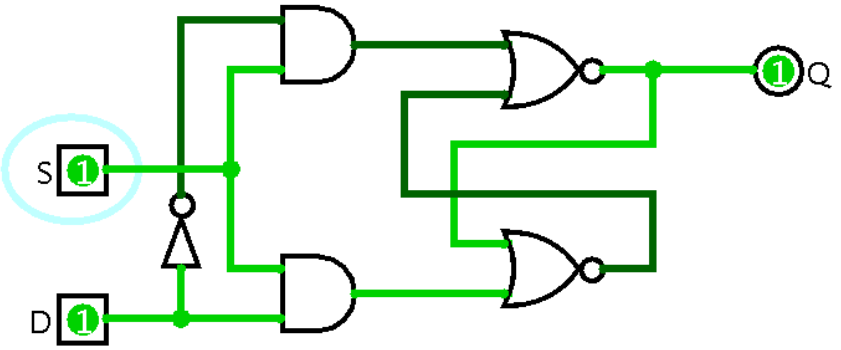
D latch





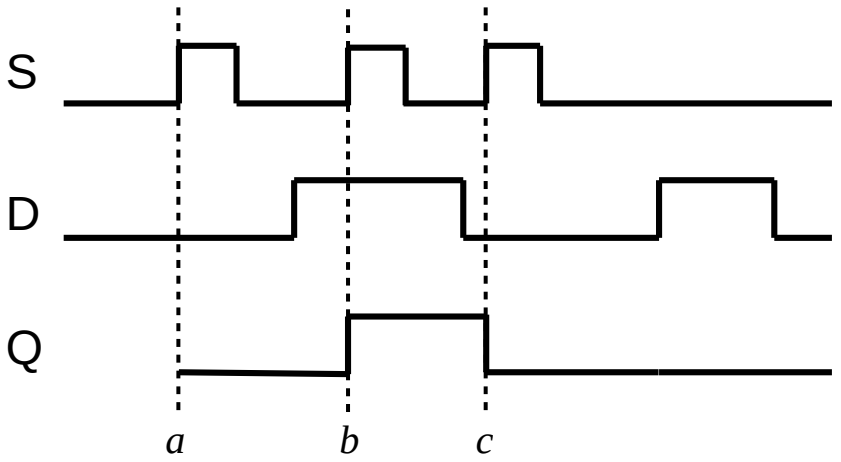
From “Code” book: S = “Save that bit!”



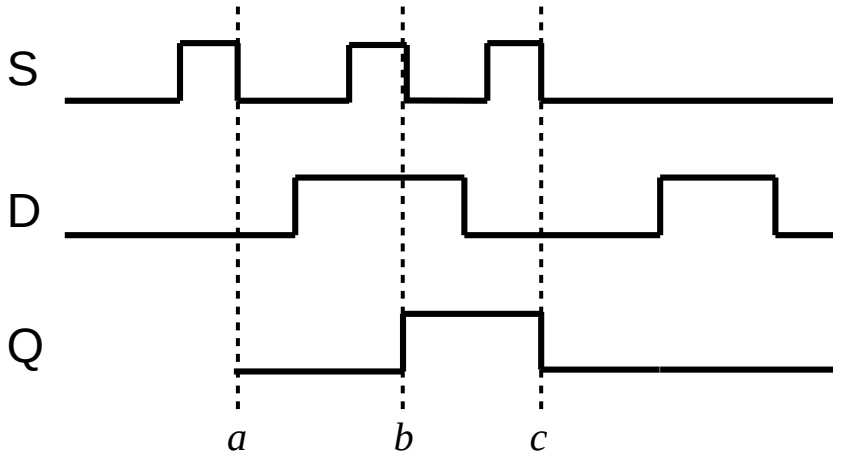


Signal changes

- Edge-triggered latches change Q on rising edge of “set” signal
- Master-slave latches change Q on falling edge of “set” signal



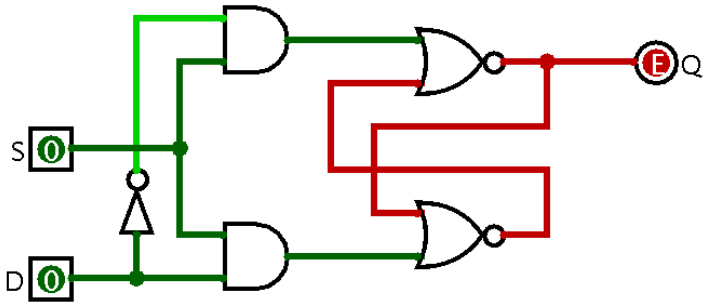
Original (edge-triggered) D latch

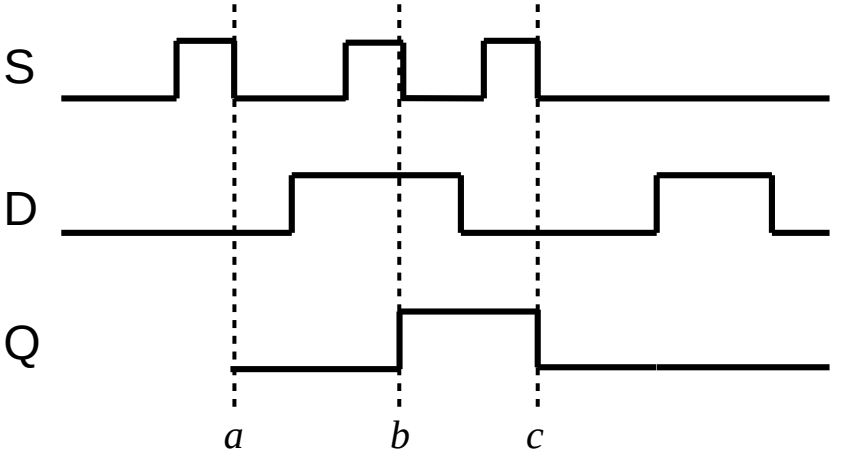


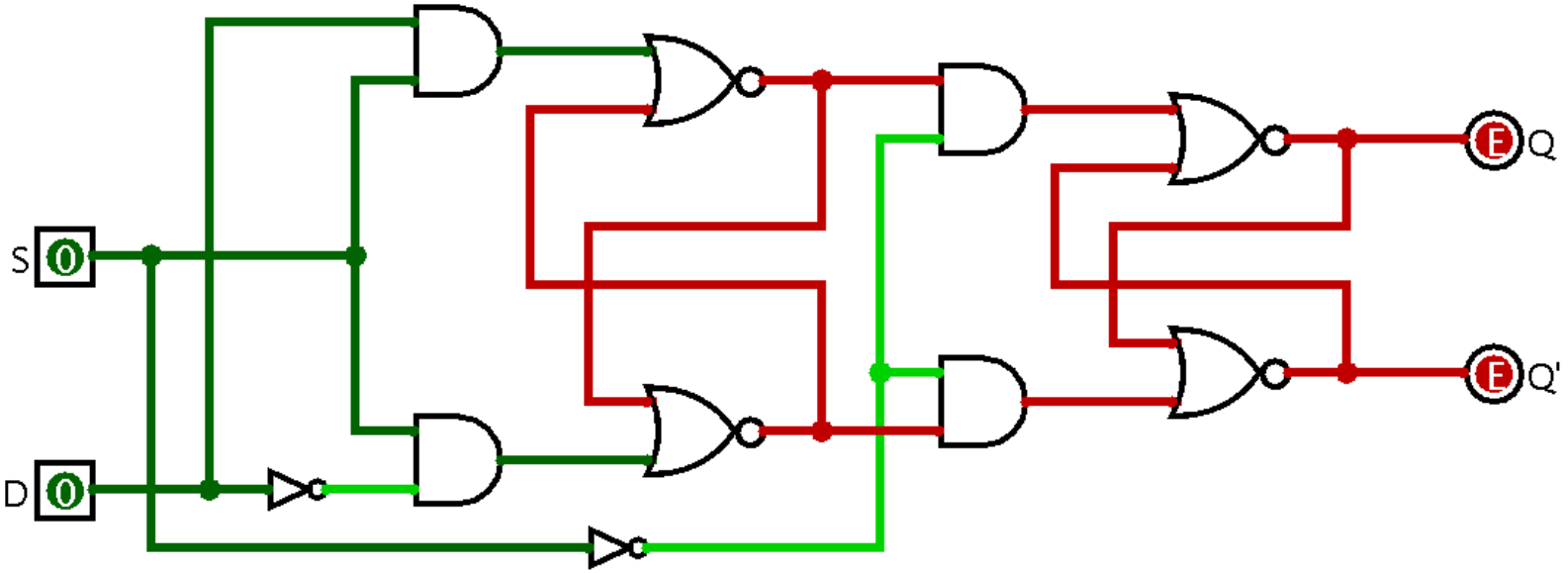
Master-slave D latch

Master-slave D latch

Original D latch:







Clocks

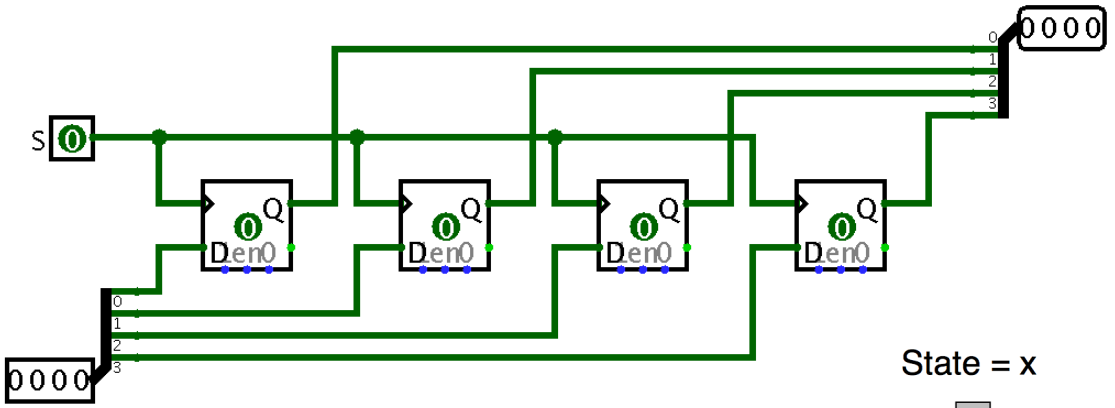
- Provide oscillating signal
- Often used as “set” signal for latches
- Keep computation and memory in sync
- Clocked latches are called flip-flops

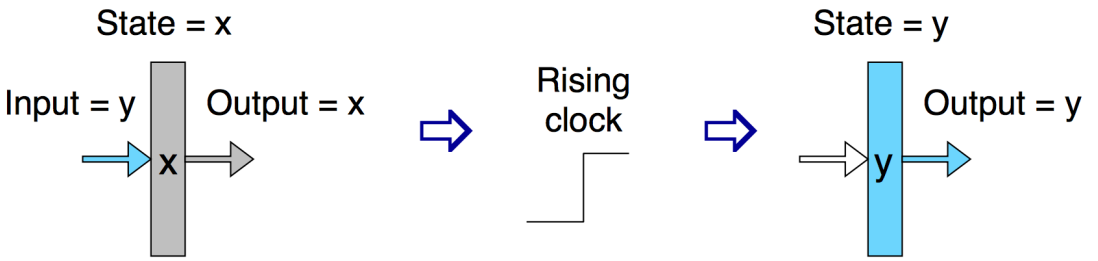
Flip-flop types

- SR: “set-reset”
- D: “data” bit + clock
- T: “toggle”
- JK: like SR + T (toggle when S=1, R=1)
  - J is S, K is R
- Any of these can be used to build the others
- Also can be built from basic logic gates in multiple ways

Registers

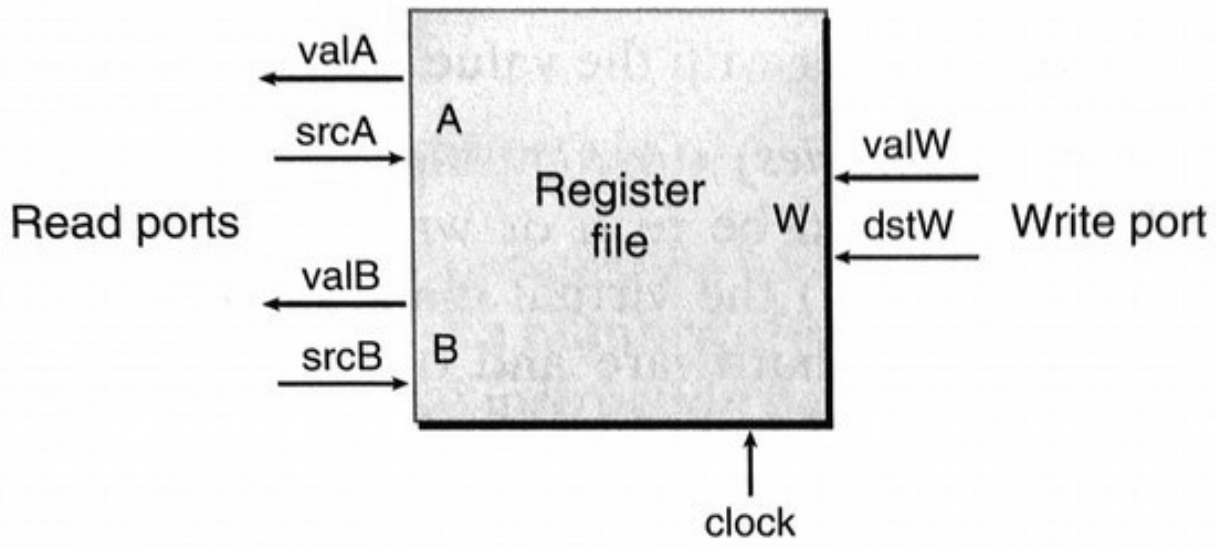
- Registers: arrays of flip-flops with a single set/clock input
- Connected by buses (groups of wires) to other components
- Edge triggering allows computation to stabilize before results are saved
- Caveat: difference between hardware registers and program registers
  - Former are physical, latter are logical (and stored in a register file)





Register files

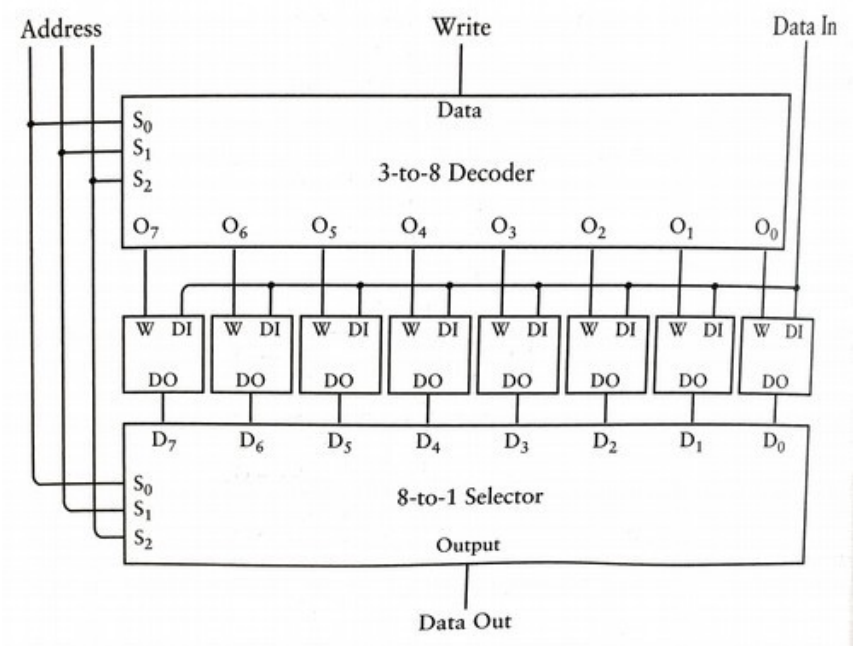
- Register files: multiple registers w/ selector inputs
  - Use multiplexors to differentiate



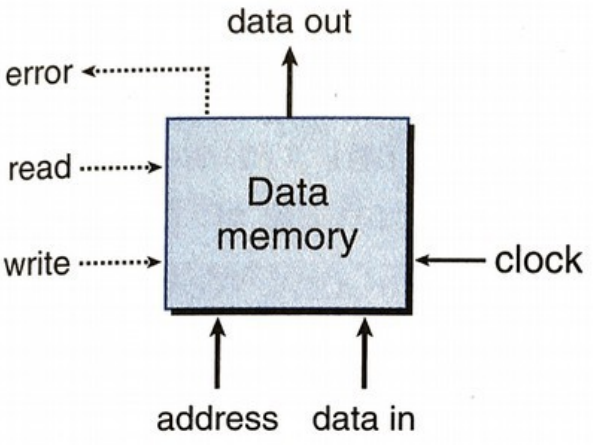
Use multiplexors to read/write from the appropriate register using srcA, srcB, or dstW signals (set dstW to 0xF to read only)

Memory

- Memory: multiple flip-flops w/ address input
  - Random access memory (RAM) - can access any address at any time
  - Use decoder (translates 3-bit number to 8 “set” signals) to write data
  - Use selector (multiplexor) to read data



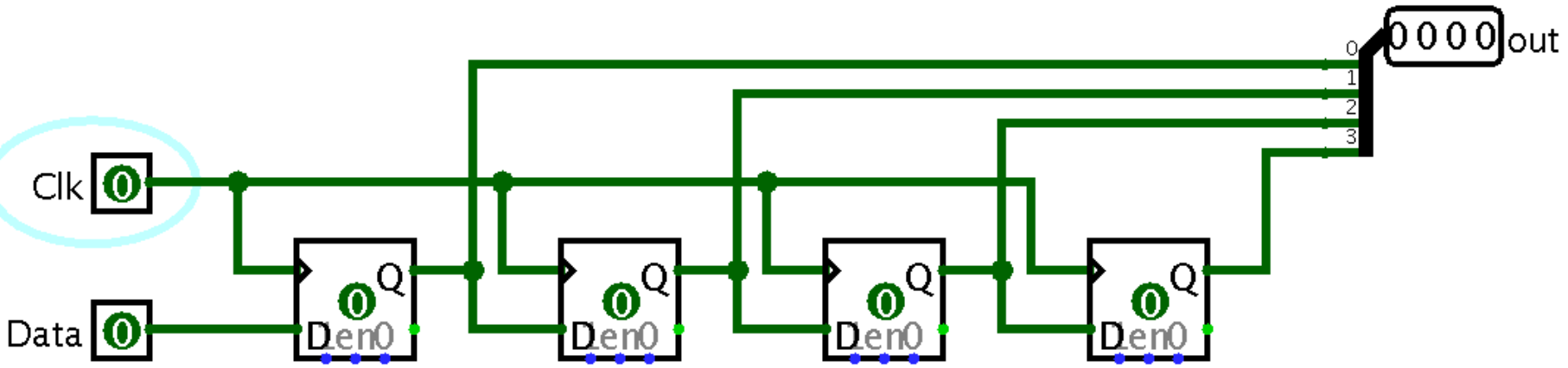
Single RAM array



Abstraction of multiple RAM arrays

Shift registers

- Uses chained flip-flops to perform bit shifts
  - Left vs. right shift
  - Serial-in vs. parallel-in



Counters

- Uses rippled flip-flops w/ feedback to count
  - Similar to adders